Code No: P18CST04

R18

HALL TICKET NUMBER

PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
(AUTONOMOUS)
II B.TECH I SEMESTER END REGULAR/SUPPLEMENTARY EXAMINATIONS, JAN - 2023
COMPUTER ORGANIZATION
(Common to AIDS,AIML Branches)

Time: 3 hours Max. Marks: 60

Note: Question Paper consists of Two parts (Part-A and Part-B)

PART-A

Answer all the questions in Part-A (5X2=10M)

Q.No.		Questions	Marks	CO	KL
1.	a)	Define Instruction code	[2M]	1	1
	b)	Discuss about Shift Micro operations	[2M]	2	6
	c)	Fixed Point Vs Floating Point representation	[2M]	3	5
	d)	Define Principle of locality	[2M]	4	1
	e)	Define Cache coherence	[2M]	5	1

PART-B

Answer One Question from each UNIT (5X10=50M)

Q.No.		Questions	Marks	CO	KL
		UNIT-I			
2.	a)	Discuss about i) Immediate ii) Direct iii) Register iv) Relative v) Auto Increment Addressing Modes	[5M]	1	6
	b)	Discuss about Memory Reference Instructions with suitable micro-operations	[5M]	1	6
		OR			
3.	a)	Discuss about Instruction cycle with flow chart	[5M]	1	6
	b)	Elaborate given expression (A+B) *(C+D) using i) Three Address ii) Two Address Instruction Formats	[5M]	1	6
		UNIT-II			
4.	a)	Construct Common Bus system consists of 4 Registers with 4 bits each using Multiplexer	[5M]	2	6
	b)	Discuss about application of Logic Microoperations	[5M]	2	6
		OR			
5.	a)	Construct 4-bit logic microoperation circuit with neat diagram	[5M]	2	6
	b)	Illustrate selection of address for control memory with neat diagram	[5M]	2	2
6.	a)	Represent the +1001.11 in floating point with 8 bit fraction and 6 bit exponent and discuss in detail	[5M]	3	5
	b)	Draw the flow chart of addition and subtraction algorithm discuss with example	[5M]	3	3
		OR			
7.	a)	Draw the flow chart of Booth multiplication algorithm with example	[5M]	3	3
	b)	Discuss the subtraction of unsigned numbers using r's complement with example	[5M]	3	6

UNIT-IV					
8.	a)	Discuss about Direct Mapping Technique used in Cache organization	[5M]	4	6
	b)	Discuss about DMA Controller with neat diagram	[5M]	4	6
OR					
9.	a)	Discuss about Daisy Chaining Priority Interrupt	[5M]	4	6
	b)	Discuss about Associate Memory	[5M]	4	6
UNIT-V					
10.	a)	Discuss about Arithmetic Pipeline	[5M]	5	6
	b)	Discuss about Symmetric Multiprocessor	[5M]	5	6
OR					
11.	a)	Discuss about Instruction Pipeline	[5M]	5	6
	b)	Discuss about Characteristics of Multi-Processor	[5M]	5	6

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